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22 Number of Pages (including this page)

Date: February 10, 2005

To: BOX AF – Mehdi Namazi – 2188

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From: David G. Dolezal - 41,711

Subject: 09/772,830– Frank K. Baker, Jr.

MESSAGE: Enclosed herewith, please find a FORMAL AMENDMENT for filing in the below-identified application.

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	x	1 page Facsimile Cover Sheet
2.	x	19 page Appeal Brief
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PAGE 1/22 * RCVD AT 2/10/2005 1:00:50 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:5129966854 * DURATION (mm-ss):08-08

In re Application of:
Frank K Baker Jr., et al.
Serial No.: 09/772,830
Filed: Jan. 30, 2001
For: A MEMORY SYSTEM AND METHOD OF ACCESSING THEREOF

February 10, 2005

Art Unit: 2188
Examiner: Mehdi Namazi
Docket No.: SC11150TH

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO: COMMISSIONER OF PATENTS AND TRADEMARKS, ALEXANDRIA, VA 22313,
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APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent.

REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin Texas.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1-4, 6-10, and 12-26 are pending.

Claim 15 has been allowed.

Claims 1-4, 6-10, 12-14, and 16-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno, U.S. Patent No. 6,105,114 (Okuno) in view of Cliff et al., U.S. Patent No. 6,392,438 (Cliff).

The rejection of claims 1-4, 6-10, and 12-26 are being appealed.

STATUS OF AMENDMENTS

There have been no amendments made to the claims subsequent to the final rejection.

SUMMARY OF THE INVENTION

Independent claim 1 recites a memory system. The memory system includes an array of addressable storage elements arranged in a plurality of rows and a plurality of columns. The array of addressable storage elements includes a plurality of nonvolatile memory cells. The memory system includes decoding circuitry coupled to the array of addressable storage elements. The decoding circuitry, responsive to decoding a first element address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second element address consecutive to the first element address, to access a second storage element of a second row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. The first address comprises a group of bits. The second address comprises a group of bits. The decoding circuitry includes a row decoder and a column decoder. The row decoder is operable responsive to a first portion of the group of bits of the first address and the second address. The column decoder is operable responsive to a

second portion of the group of bits of the first address and the second address. A bit of the second portion is more significant than a bit of the first portion.

In one example set forth in the specification of the present application, the memory system includes an array (210) of addressable storage elements (212) arranged in a plurality of rows and a plurality of columns. See Figure 2. The array of addressable storage elements includes a plurality of nonvolatile memory cells. Page 3, lines 18-19. The memory system includes decoding circuitry coupled to the array of addressable storage elements. (230, 220) The decoding circuitry, responsive to decoding a first element address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second element address consecutive to the first element address, to access a second storage element of a second row of the plurality of rows. Page 3, line 29 – page 4, line 9. The second row of the plurality of rows is different from the first row of the plurality of rows. The first address comprises a group of bits. The second address comprises a group of bits. The decoding circuitry includes a row decoder (230) and a column decoder (220). The row decoder is operable responsive to a first portion of the group of bits (the bits of A0 and A1) of the first address and the second address. The column decoder is operable responsive to a second portion of the group of bits (the bits of A2 and A3) of the first address and the second address. A bit of the second portion is more significant than a bit of the first portion. See Figure 2 and page 3, line 14 - page 4 line 9.

Claim 6 recites a memory system. The memory system includes an array of storage elements arranged in a plurality of rows and a plurality of columns. Each of the storage elements includes an input and an output. Each of the storage elements corresponds to a numeric address comprising more significant bits and less significant bits. The array of storage elements comprises a plurality of nonvolatile memory cells. The memory system includes a column decoder coupled to the outputs of the storage elements of each of the plurality of columns. The column decoder is operable responsive to at least one of the more significant bits. The memory system includes a row decoder coupled to the inputs of the storage elements of each of the plurality of rows. The row decoder is operable responsive to at least one of the less significant bits.

In one example set forth in the specification of the present application, the memory system includes an array (210) of storage elements (212) arranged in a plurality of rows and a plurality of columns. See Figure 2. Each of the storage elements includes an input and an output. Page 10, lines 4-6. Each of the storage elements corresponds to a numeric address comprising more significant bits and less significant bits. Page 3, lines 19-28. The array of storage elements comprises a plurality of nonvolatile memory cells. Page 3, lines 17-19. The memory system includes a column decoder (220) coupled to the outputs of the storage elements of each of the plurality of columns. The column decoder is operable responsive to at least one of the more significant bits (the bits of A2 and A3). The memory system includes a row decoder (230)

coupled to the inputs of the storage elements of each of the plurality of rows. The row decoder is operable responsive to at least one of the less significant bits (the bits of A1 and A2).

Claims 14 recites an embedded control system. The control system includes a processor and a memory system coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. The control system includes decoding circuitry including a column decoder and a row decoder. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. Each address includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. A bit of the second portion is more significant than a bit of the first portion.

In one example set forth in the specification of the present application, the embedded control system (300) includes a processor (301) and a memory system (302) coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks (BLK1 and BLK2). Page 4, lines 11-14. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Page 5, lines 4-11. The control system includes decoding circuitry including a column decoder 320 and a row decoder (330). The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. See Figure 3. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. See Figure 3. Page 5, line 12- page 6, line 2. Each address includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. Page 5, line 12 – page 6, line 2. A bit of the second portion is more significant than a bit of the first portion. See Figure 7 and page 6, lines 8-28.

Claim 16 recites a method of accessing a memory system. The memory system includes an array of addressable storage elements arranged in a plurality of rows and a plurality of columns. The array of addressable storage elements includes a plurality of nonvolatile memory cells. The method includes decoding a first element address. The method also includes accessing, responsive to the first element address, a first storage element of a first row of the plurality of rows. The method also includes decoding a second element address, the second element address consecutive to the first element address. The method still further includes accessing, responsive to the second element address, a second storage element of a second row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. The first element address includes a group of bits. The decoding the first element address further includes decoding a first portion of the group of bits by a row decoder and decoding a second portion of the group of bits by a column decoder. A bit of the second portion is more significant than a bit of the first portion.

In one example set forth in the specification of the present application, the memory system includes an array (210) of addressable storage elements (212) arranged in a plurality of rows and a plurality of columns. The array of addressable storage elements includes a plurality of nonvolatile memory cells. Page 3, lines 17-19. The method includes decoding a first element address. The method also includes accessing, responsive to the first element address, a first storage element of a first row of the plurality of rows. The method also includes decoding a second element address, the second element address consecutive to the first element address. The method still further includes accessing, responsive to the second element address, a second storage element of a second row of the plurality of rows. The second row of the plurality of rows is different from the first row of the plurality of rows. Page 3, line 29 - page 4, line 3. The first element address includes a group of bits. The decoding the first element address further includes decoding a first portion of the group of bits (the bits of A0 and A1) by a row decoder (230) and decoding a second portion of the group of bits (the bits of A2 and A3) by a column decoder (220). A bit of the second portion is more significant than a bit of the first portion.

Claim 22 recites an embedded control system. The control system includes a processor and a memory system coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. The control system includes decoding circuitry including a column decoder and a row decoder. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having

a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. The address signal includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. Each bit of the second portion is more significant than a least significant bit of the first portion.

In one example set forth in the specification of the present application, the embedded control system (300) includes a processor (301) and a memory system (302) coupled to the processor. The memory system includes an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks (BLK1 and BLK2). Page 4, lines 11-14. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Page 5, lines 4-11. The control system includes decoding circuitry including a column decoder 320 and a row decoder (330). The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. See Figure 3. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. See Figure 3 and page 5, line 12 – page 6, line 2. The address signal includes a group of bits. The row decoder is operable responsive to a first portion of the group of bits. The column decoder is operable responsive to a second portion of the group of bits. Page 5, line 12 – page 6, line 2. Each bit of the second portion is more significant than a least significant bit of the first portion. See Figure 7 and page 6, lines 8-28.

Claim 25 recites a memory system that includes an input to receive an address signal, an output to send addressed information, and a plurality of blocks. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Each of the plurality of blocks includes decoding circuitry including a column decoder and a row decoder. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. The address signal includes a first

group of bits representative of addresses of the plurality of rows and a second group of bits representative of addresses of pages within the plurality of rows. The second group includes a bit more significant than a bit of the first group. The address signal includes a third group of at least one bit representative of addresses of the plurality of blocks.

In one example set forth in the specification of the present application, the memory system includes an input to receive an address signal, an output to send addressed information, and a plurality of blocks. See Figure 3 and page 4, lines 10-14 and lines 25-30. Each of the plurality of blocks includes an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages. Page 4, lines 10-25 and page 5, lines 4-11. Each of the plurality of pages includes a plurality of words. Each of the plurality of words includes a plurality of bits. Page 5, lines 4-11. Each of the plurality of blocks includes decoding circuitry including a column decoder and a row decoder. Figure 3. The decoding circuitry is coupled to the input, the output and the array of nonvolatile memory cells. See Figure 3. The decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows. The decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output. Page 5, line 12 – page 6, line 7. The address signal includes a first group of bits representative of addresses of the plurality of rows and a second group of bits representative of addresses of pages within the plurality of rows. See Figure 7 and page 6, lines 8-28. The second group includes a bit more significant than a bit of the first group. The address signal includes a third group of at least one bit representative of addresses of the plurality of blocks. See Figure 7 and page 6, lines 8-28.

The specification and drawings may contain other embodiments of the claims not explicitly set forth above.

GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 1-4, 6-10, 12-14, and 16-26 obvious under 35 U.S.C. 103(a) as being unpatentable over Okuno, U.S. Patent No. 6,105,114 (Okuno) in view of Cliff et al., U.S. Patent No. 6,392,438 (Cliff).

ARGUMENTS

Arguments for Ground 1

Independent Claim 1

Claim 1 is non obvious over Okuno and Cliff in that the Final Office Action has failed to set forth a proper motivation to replace the memory circuit of Okuno with a ROM of Cliff to teach the limitations of claim 1. Accordingly, the Final Office Action has not set forth a prima facie case for Obviousness of claim 1.

Final Office Action Rejection

Claim 1 was rejected in Section 3 of the Final Office Action. Section 3 states that Okuno fails to teach a storage with a plurality of nonvolatile memory cells.

Section 3 of the Final Office Action states that Cliff discloses a storage with plurality of memory cell array, wherein data could be read or written as a ROM array. In this way Cliff teaches a storage with plurality of nonvolatile memory cells, in order to preserved data from erasure.

Section 3 of the Final Office Action further states that "it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use a nonvolatile memory, wherein nonvolatile memory is able to conserve data even when there is no power supply, as taught by Cliff into [the] system of Okuno in order to preserve data from erasure in case of [a] power shortage. One of ordinary skill in the art would found ample suggestion therein to modify the Okuno system by providing a plurality of nonvolatile memory cells, where each memory cell can preserve one bit of data in event of power failure."

No Motivation To Combine

Applicants respectfully submit that claim 1 is allowable over Okuno and Cliff in that one of ordinary skill in the art would not have been motivated to use the circuitry of Cliff configured as a ROM in the circuit of Okuno for at least the reasons given below.

Combination Renders Okuno Unsatisfactory for Intended Purpose

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, there is no suggestion or motivation to make the proposed modification." MPEP Section 2143.01, Subsection THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE.

One of ordinary skill in the art would not be motivated to replace memory circuit 2 of Okuno with a ROM array as stated as taught in Cliff in that the circuit of Okuno could not perform its stated purpose with such a modification.

Okuno teaches a transposition circuit for implementing a transforming coding technique using a two-dimensional discrete cosine transform for coding image data such as MPEG data. Okuno, column 1, lines 8-25. More specifically, Okuno discloses a transposition memory circuit 1 used for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT). Okuno, column 1, lines 8-25, column 4, lines 5-9, and column 7, lines 31-47. The circuit of Okuno is used for decoding multiple blocks of image data with a read and write operation being performed to each cell of a

memory cell array 2 of memory circuit 1 for each block of data being processed. Okuno, column 7, line 31- column 8, line 36. The circuit of Okuno performs these functions by reading data in array 2 in an order different from writing data to the array. Okuno, column 1, lines 8-10.

For memory cell array 2 of Okuno, data can be written to and read from simultaneously and independent of each other. Okuno, column 10, lines 1-6. Accordingly, when the reading of data (e.g. one pixel) from a cell for a first block of data (of NxN pixel data) is complete, data from a next block of data can be written to the cell. See Okuno, column 9, line 51 to column 10, line 16 where it describes how data from a first block (data that was previously written) is read from the memory cells of array 2 while data from a second block is written to the memory cells of array 2. See also Okuno, column 10, lines 17 to column 10, line 34 where it describes how data from the second block is read from the memory cells of array 2 while data from a third block is written to the memory cells. For accomplishing these operations, memory cell array 2 is responsive to a clock signal for writing data to a memory cell at a rising edge of a clock signal and reading data from a memory cell at a falling edge of a clock signal. Okuno, column 7, lines 48-66.

Accordingly, for the circuit of Okuno to perform its intended purposes, the cells of its memory array need to be written to simultaneously with reads to the cells and need to be written to multiple times for performing transforms on image data.

The ability to perform the operations above enables circuit 1 to perform the transportations of a two dimension array of data with one memory cell array and without using two memory cell arrays. Okuno column 4, lines 32-40; column 5, lines 5-12; column 5, lines 40-42; column 6, lines 6-9 and lines 50-52; and column 11, lines 27-35. The ability to perform these operations without two memory arrays is enabled by the use of a memory array having memory cells that can be written to and read from simultaneously. See Okuno, Column 5, lines 25-27 and lines 44-46; column 6, lines 10-14 and lines 51-54; column 8, lines 37-40; and column 10, lines 1-6. The ability of circuit 1 of Okuno to perform the desired operations without two memory arrays results in reducing circuit scale and power consumption. Okuno, column 4, lines 38-40; column 5, lines 12-14; column 6, lines 21-23 and lines 56-58; and column 11, lines 31-36. Also, such a memory array enables the circuit to have the same processing speed as conventional circuitry. See Okuno, column 5, lines 47-49; column 6, lines 14-15 and lines 24-26, and column 6, lines 54-56.

Cliff teaches a programmable logic array integrated circuit device. See Abstract of Cliff. Cliff teaches that its circuitry can be programmed to implement logic devices such as AND, NAND, OR, or NOR circuits (Column 7, line 27) and can be programmed to perform adder and counter functions (Column 5, lines 63-64).

Section 3 of the Final Office Action states with regard to Cliff that "data could be read or written as a ROM array."

One of ordinary skill in the art would not be motivated to replace memory circuit 2 of Okuno with a ROM array as stated as taught in Cliff in that the circuit of Okuno could not perform its stated purpose (a transposition memory circuit 1 used for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT)) utilizing a ROM (read only memory) in place of memory circuit 2 of Okuno.

As stated above, Okuno requires that for memory circuit 2, data is to be written to and read from simultaneously and independent of each other during circuit operation and that data is to be written to the cells of memory circuit 2 multiple times during circuit operation.

If the programmable logic array of Cliff is programmed as a ROM (read only memory), then data can not be written to that ROM. Accordingly, one of ordinary skill in the art would not replace memory circuit 2 of Okuno with a ROM as taught by Cliff in that data could not be written to the ROM and therefore the circuit of Okuno could not perform the transposition operations.

See for example, Column 17, lines 8-10 of Cliff where it states that if the RAM regions act like a ROM, "the read-write control signal is held permanently high to force the memory into read mode only." If the circuit of Cliff is programmed as a ROM and implemented into Okuno, then Okuno could not perform its stated purpose because the read-write control signal would be permanently high, preventing data from being written into the ROM. Thus, without the ability to write data into its memory, the circuitry of Okuno can not perform the function of transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT) for such functions as processing image data.

Therefore, one of skill in the art could not implement circuit 1 of Okuno with the circuit of Cliff programmed as a ROM in that memory circuit 1 of Okuno modified to include a ROM in place of memory circuit 2 could not perform the transposition operations as set forth in Okuno in that data could not be written to the ROM to perform those operations. See also MPEP Section 2143.01, Subsection entitled THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF A REFERENCE.

Stated Motivation to Combine is Deficient

Section 3 of the Final Office Action states that one of skill in the art would have been motivated to use the memory taught by Cliff in the system of Okuno in order to preserve data from erasure in case of a power shortage. Applicants respectfully submit that this reason would not motivate one of skill in the art to combine the circuit of Cliff programmed as a ROM in the system of Okuno.

First, Okuno teaches a transposition circuit for implementing a transforming coding technique using a two-dimensional discrete cosine transform for coding image data such as MPEG data. Okuno, column 1, lines 8-25. Okuno implements a transposition memory circuit 1 for performing these operations. Okuno, column 7, lines 31-47. The circuit of Okuno is used for

decoding multiple blocks of image data with a read and write operation being performed to each cell of array 2 for each block of data being processed. Okuno, column 7, line 31- column 8, line 36.

Nowhere in Okuno does it require circuit 1 of Okuno to be able to store data when the power is off, nor is there any suggestion of it being desirable to save the data in memory array 2. In fact, memory array 2 is not utilized to store data for any substantial period of time. Okuno appears to teach that data is only "stored" in memory array 2 during a cycling of the addresses as provided by counter 20 to perform the transposition operations. See Okuno, column 8, lines 9-13 and in general column 9, line 31 – column 10, line 34. Since circuit 1 is part of a coding system for image data, there is no need to store data in array 2 when circuit 1 does not have power in that circuit 1 would not be used to encode data when there is no power. Because there is no need to store data in array 2 of Okuno (other than for a short period of time during a transposition operation), there is no reason for one of skill in the art to modify Okuno to include the circuit of Cliff programmed to be a ROM for the purpose of saving data during a power outage.

Claim 1 Summary

Accordingly, because 1) Okuno teaches that its systems uses an array in which data can be written to and read from simultaneously and independently of each other, and the circuit of Cliff programmed to be ROM can not meet this requirement and 2) because the ability to save the data in memory array 2 of Okuno during a power outage is not a requirement or even desirable, one of skill in the art would not be motivated to modify the circuit of Okuno with the logic array of Cliff programmed as a ROM. Accordingly, amended claim 1 is allowable over Okuno and Cliff.

Independent Claim 6

For reasons similar to those set forth above for independent claim 1, independent claim 6 is non obvious over Okuno and Cliff in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Cliff to teach the limitations of independent claim 6. Accordingly, independent claim 6 is allowable over Okuno and Cliff.

Independent Claim 14

For reasons similar to those set forth above for independent claim 1, independent claim 14 is non obvious over Okuno and Cliff in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Cliff to teach the limitations of independent claim 14. Accordingly, independent claim 14 is allowable over Okuno and Cliff.

Independent Claim 16

For reasons similar to those set forth above for independent claim 1, independent claim 16 is non obvious over Okuno and Cliff in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Cliff to teach the limitations of independent claim 16. Accordingly, independent claim 16 is allowable over Okuno and Cliff.

Independent Claim 22

For reasons similar to those set forth above for independent claim 1, independent claim 22 is non obvious over Okuno and Cliff in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Cliff to teach the limitations of independent claim 22. Accordingly, independent claim 22 is allowable over Okuno and Cliff.

Independent Claim 25

For reasons similar to those set forth above for independent claim 1, independent claim 25 is non obvious over Okuno and Cliff in that the Final Office Action has failed to set forth a proper motivation to combine Okuno and Cliff to teach the limitations of independent claim 25. Accordingly, independent claim 25 is allowable over Okuno and Cliff.

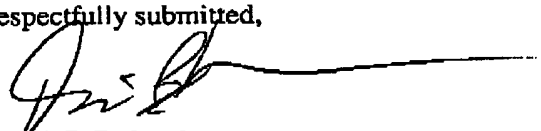
Dependent claims 2-4, 7-10, 12, 13, 17-21, 23, 24, and 26

Each dependent claim depends from an independent claim and is allowable for at least this reason.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the claims of the present application are allowable over the art cited during prosecution.

Respectfully submitted,



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Claims Appendix

1. (Previously Amended) A memory system comprising:

an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells; and

decoding circuitry coupled to the array of addressable storage elements, the decoding circuitry, responsive to decoding a first element address, to access a first storage element of a first row of the plurality of rows, and the decoding circuitry, responsive to decoding a second element address consecutive to the first element address, to access a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows;

wherein the first address comprises a group of bits;

wherein the second address comprises a group of bits;

wherein the decoding circuitry includes a row decoder and a column decoder;

wherein the row decoder is operable responsive to a first portion of the group of bits of the first address and the second address;

wherein the column decoder is operable responsive to a second portion of the group of bits of the first address and the second address, wherein a bit of the second portion is more significant than a bit of the first portion.

2. (Original) A memory system according to claim 1 wherein each of the storage elements stores one bit.

3. (Original) A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a word.

4. (Original) A memory system according to claim 1 wherein each of the storage elements stores a plurality of bits arranged as a page.

5. (Canceled).

6. (Previously Amended) A memory system comprising:

an array of storage elements arranged in a plurality of rows and a plurality of columns, each of the storage elements comprising an input and an output, each of the storage elements corresponding to a numeric address comprising more significant bits and less significant bits, wherein the array of storage elements comprises a plurality of nonvolatile memory cells;

a column decoder coupled to the outputs of the storage elements of each of the plurality of columns, the column decoder operable responsive to at least one of the more significant bits; and

a row decoder coupled to the inputs of the storage elements of each of the plurality of rows, the row decoder operable responsive to at least one of the less significant bits.

7. (Original) A memory system according to claim 6 wherein
the input of each of the storage elements is a control gate, and
the output of each of the storage elements is a drain.

8. (Original) A memory system according to claim 6 wherein each of the storage elements stores one bit.

9. (Original) A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a word.

10. (Original) A memory system according to claim 6 wherein each of the storage elements stores a plurality of bits arranged as a page.

11. (Canceled)

12. (Original) A memory system according to claim 6 wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell.

13. (Original) A memory system according to claim 6 wherein the at least one of the less significant bits comprises all of the less significant bits.

14. (Previously Amended) An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein each address comprises a group of bits;

wherein the row decoder is operable responsive to a first portion of the group of bits;

wherein the column decoder is operable responsive to a second portion of the group of bits, wherein a bit of the second portion is more significant than a bit of the first portion.

15. (Previously Amended) An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of

pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein the address signal comprises:

least significant bits representative of addresses of bits within a word,

next least significant bits representative of addresses of words within a page,

intermediate significant bits representative of addresses of the plurality of rows, the intermediate significant bits more significant than the next least significant bits,

more significant bits representative of addresses of pages within the plurality of rows, the more significant bits more significant than the intermediate significant bits, and

next more significant bits representative of addresses of the plurality of blocks, the next more significant bits more significant than the more significant bits.

16. (Previously Amended) A method of accessing a memory system, the memory system comprising an array of addressable storage elements arranged in a plurality of rows and a plurality of columns, wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells, the method comprising:

decoding a first element address;

accessing, responsive to the first element address, a first storage element of a first row of the plurality of rows;

decoding a second element address, the second element address consecutive to the first element address; and

accessing, responsive to the second element address, a second storage element of a second row of the plurality of rows, the second row of the plurality of rows different from the first row of the plurality of rows;

wherein the first element address includes a group of bits;

wherein the decoding the first element address further includes decoding a first portion of the group of bits by a row decoder and decoding a second portion of the group of bits by a column decoder;

wherein a bit of the second portion is more significant than a bit of the first portion.

17. (Original) A method according to claim 16 wherein accessing a first storage element comprises reading a first page, the first page comprising a plurality of bits.

18. (Original) A method according to claim 17 wherein accessing a second storage element comprises reading a second page different from the first page, the second page comprising a plurality of bits.

19. (Original) A method according to claim 16 wherein accessing a first storage element comprises initiating a first burst access, the first burst access comprising a plurality of bits.

20. (Original) A method according to claim 19 wherein accessing a second storage element comprises initiating a second burst access different from the first burst access, the second burst access comprising a plurality of bits.

21. (Previously Added) The memory system of claim 6 wherein:

the numeric address comprises a group of bits;

the row decoder is operable responsive to a first portion of the group of bits;

the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.

22. (Previously amended) An embedded control system comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an input to receive an address signal from the processor, an output to send addressed

information to the processor, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein:

the address signal comprises a group of bits;

the row decoder is operable responsive to a first portion of the group of bits;

the column decoder is operable responsive to a second portion of the group of bits, wherein each bit of the second portion is more significant than a least significant bit of the first portion.

23. (Previously added) The memory system of claim 1 wherein each bit of the second portion is more significant than a least significant bit of the first portion.

24. (Previously added) The method of claim 16 wherein each bit of the second portion is more significant than a least significant bit of the first portion.

25. (Previously added) A memory system comprising an input to receive an address signal, an output to send addressed information, and a plurality of blocks, each of the plurality of blocks comprising:

an array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns to store information within a plurality of pages, each of the plurality of pages comprising a plurality of words, each of the plurality of words comprising a plurality of bits; and

decoding circuitry comprising a column decoder and a row decoder, the decoding circuitry coupled to the input, the output and the array of nonvolatile memory cells, the decoding circuitry, responsive to the address signal having a first page address, accessing a first page of a first row of the plurality of rows, the decoding circuitry, responsive to the address signal having a second page address consecutive to the first page address, accessing a second page of a second row of the plurality of rows, and, thereafter, the decoding circuitry coupling the first and second pages to the output;

wherein the address signal comprises:

a first group of bits representative of addresses of the plurality of rows,

a second group of bits representative of addresses of pages within the plurality of rows, wherein the second group includes a bit more significant than a bit of the first group;

a third group of at least one bit representative of addresses of the plurality of blocks.

26. (Previously added) The embedded control system of claim 14, wherein at least one bit of the group of bits is representative of addresses of the plurality of blocks.

FEE TRANSMITTAL

Patent fees are subject to annual revision

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500

Complete if Known	
Application Number	09/772,830
Filing Date	January 30, 2001
First Named Inventor	Frank K. Baker, Jr.
Examiner Name	Mehdi Namazi
Group Art Unit	2188
Attorney Docket No.	SC11150TH

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 503079

Deposit Account Name: Freescale Semiconductor, Inc.

The Director is authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fees(s) indicated below, except for the filing fee to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)		Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	780	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Previously Paid**		Extra Claims		Fee from below		Fee Paid
Total Claims	24	- 20	= 24	X	18	=	0
Independent Claims	7	- 6	= 1	X	86	=	86
Multiple Dependent					280	=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	* Reissue independent claims over original patent
1205	18	2205	9	*Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late Provisional filing	
1053	130	1053	130	Non-English specification	
1812	2520	1812	2520	For filing a request for ex parte Reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1840*	1805	1840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1480	2254	740	Extension for reply within fourth month	
1255	2010	2255	1005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	500	2402	165	Filing a brief in support of an appeal	500
1403	290	2403	145	Request for oral hearing	
1451	1510	1451	1510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1330	2453	665	Petition to revive – unintentional	
1501	1330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of IDS	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

SUBTOTAL (3) ($) 500

* Reduced by Basic Filing Fee Paid

SUBMITTED BY

Complete (if applicable)

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